wherein the conductive posts are electrically connected to the interconnecting pattern through the conductive particles.

7. (Twice Amended) A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern,

wherein a recognition hole is formed in the substrate at a position differing from the holes; and

wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern.

10. (Twice Amended) The semiconductor device as defined in claim 1, wherein the conductive posts are a plurality of layered bumps.

13. (Amended) A semiconductor device comprising:

a substrate including a plurality of holes and a surface over which an interconnecting pattern is formed, part of the interconnecting pattern being superposed over the holes;

a semiconductor chip disposed over another surface of the substrate and including a plurality of electrodes to be positioned over the holes; and

conductive members provided within the holes for electrically connecting the electrodes to the interconnecting pattern,

wherein the conductive members are a plurality of layered bumps,

wherein the bumps include first bumps formed on the electrodes and second bumps formed on the first bumps,